

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1. (Currently Amended) A memory card having a plurality of non-volatile memories and a memory controller for controlling operation of said plurality of non-volatile memories, wherein

said memory controller performs an access control of said plurality of non-volatile memories in response to an external access instruction, and an alternation control for substituting a storage area of an access error-related non-volatile memory with another storage area;

each of said plurality of non-volatile memories includes a plurality of sectors, a first sector of which stores management information used for performing said alternation control thereon, said alternation control being performed individually for each of said plurality of non-volatile memories; and

said memory controller causes said plurality of non-volatile memories to operate for parallel access in said access control, and issues addresses, of which a first address

is for a first non-volatile memory and a second address is for a second non-volatile memory,

wherein said memory controller controls ~~access to a first~~ issuing said addresses, such that said first address of a first non-volatile memory and said first second address of a second non-volatile memory indicate same location sectors, when both of said ~~first address sector~~ of said first non-volatile memory indicated by said first address and said first address of sector of said second non-volatile memory indicated by said second address are valid, and

wherein said memory controller controls ~~access to a second~~ issuing said addresses, such that said first address of said first non-volatile memory and a third address of said second address said second non-volatile memory indicate different location sectors, when said ~~second address sector~~ of said first non-volatile memory indicated by said first address is valid and a sector of said second non-volatile memory on same location of said sector of said first non-volatile memory indicated by said first address is invalid.

2. (Currently Amended) A memory card having first and second non-volatile memories and a ~~main-memory~~ controller for controlling operation of said first and second non-volatile memories, wherein

said memory controller allocates said first and second non-volatile memories to storage areas of even and odd data of sector data, respectively;

each of said first and second non-volatile memories has a plurality of sectors, a first sector of which stores management information used for performing an alternation control thereon, said alternation control being performed individually for each of said first and second non-volatile memories;

said memory controller causes said first and second non-volatile memories to operate for parallel access in an access control of said first and second non-volatile memories in response to an external access instruction; and

said memory controller substitutes a storage area of the access error-related non-volatile memory with another storage area in said alternation control of said first and second non-volatile memories, and issues addresses, of which a first address is for a first non-volatile memory and a second address is for a second non-volatile memory,

wherein said memory controller controls ~~access to a first~~ issuing addresses, such that said first address of said first non-volatile memory and said first-second address of said second non-volatile memory indicating indicate same location sectors, when both of said ~~first address sector~~ of said first non-volatile memory indicated by said first address and said

second address sector of said second non-volatile memory indicated by said second address do not include an error memory cell, and

wherein said memory controller controls ~~access to a~~ second issuing addresses, such that ~~said first address of said first non-volatile memory and a third address of said second address~~ said second non-volatile memory indicate different location sectors, when ~~said third address sector of said first non-volatile memory does not include an error memory cell and a sector of said second non-volatile memory on same location of said sector of said first non-volatile memory indicated by said first address~~ includes an error memory cell.

3. (Original) A memory card as defined in Claim 1, further comprising buses for connecting respective non-volatile memories to said memory controller so that said respective non-volatile memories are separately access-controlled.

4. (Previously Presented) A memory card as defined in Claim 1, wherein:

said memory controller includes an ECC circuit for adding an error detection code to write-data written into said plurality of non-volatile memories to conduct an error detection and correction for read-data from said plurality of non-volatile memories; and

said ECC circuit conducts an input/output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of the parallel access operations.

5. (Previously Presented) A memory card as defined in Claim 1, wherein:

said memory controller includes one or more ECC circuits which add an error detection code to write-data written into said plurality of non-volatile memories and conduct an error detection and correction for read-data from said plurality of non-volatile memories, said one or more ECC circuits being as many as the number of the parallel access operations; and

said one or more ECC circuits perform input/output operations in a parallel manner at an operation frequency which is equal to the input/output operation frequency of said parallel access operated non-volatile memories.

6 - 7. (Cancelled)

8. (Currently Amended) A memory controller comprising:  
a host interface circuit capable of being input/output operated in accordance with a predetermined protocol;

a memory interface circuit capable of ~~be~~being connected to a plurality of non-volatile memories in parallel; and

a control circuit connected to said host interface circuit and said memory interface circuit,

wherein said control circuit fetches a plurality of management information from said plurality of non-volatile memories, respectively, performs an external interface control via said host interface circuit, an access control of said non-volatile memories via said memory interface circuit responsive to an external access instruction, and an alternation control for substituting a storage area of an access error-related non-volatile memory with another storage area, and causes said plurality of non-volatile memories to parallel access operate in said access control by issuing addresses, of which a first address is for a first non-volatile memory and a second address is for a second non-volatile memory,

wherein said control circuit is capable of ~~accessing a first~~ issuing said addresses, such that said first address of a first non-volatile memory and said first second address of a second non-volatile memory indicate same location sectors in parallel, when both of said ~~first address sector~~ of said first non-volatile memory indicated by said first address and said first address sector of said second non-volatile memory indicated by said second address are valid, and

wherein said control circuit is capable of ~~accessing a second~~ issuing said addresses, such that said first address

address of said first non-volatile memory and a third and said second address of said second non-volatile memory in indicate different location sectors, when said ~~second address~~ sector of said first non-volatile memory indicated by said first address is valid and a sector of said second non-volatile memory on same location of said sector of said first non-volatile memory indicated by said first address is invalid.

9. (Currently Amended) A memory controller comprising:

a host interface circuit capable of being input/output operated in accordance with a predetermined protocol;

a memory interface circuit capable of being connected to first and second non-volatile memories in parallel; and

a control circuit connected to said host interface circuit and said memory interface circuit,

wherein said memory controller allocates said first and second non-volatile memories to storage areas of even and odd data of sector data, respectively, fetches first and second management information from said first and second non-volatile memories, respectively, and uses said first and second management information in an alternation control of said first and second non-volatile memories, respectively, causes said first and second non-volatile memories to parallel access operate in an access control of said non-volatile memories in

response to an external access instruction by issuing  
addresses, of which a first address is for said first non-  
volatile memory and a second address is for said second non-  
volatile memory, and substitutes storage areas for storage  
 areas in the non-volatile memory in which an access error  
 occurs in the alternation control of said first and second  
 non-volatile memories,

wherein said memory controller is capable of ~~accessing a~~  
~~first~~ issuing said addresses, such that said first address  
~~address of said first non-volatile memory and said first and~~  
~~said second address of said second non-volatile memory in~~  
indicate same location sectors, when both of said first  
~~address sector of said first non-volatile memory indicated by~~  
said first address and said first address sector of said  
second non-volatile memory indicated by said second address do  
 not include an error memory cell, and

wherein said memory controller is capable of ~~accessing a~~  
~~second~~ issuing addresses, such that said first address of said  
~~first non-volatile memory and a third said second address of~~  
~~said second non-volatile memory in parallel~~ indicate different  
location sectors, when said ~~third address sector of said first~~  
non-volatile memory indicated by said first address does not  
include an error memory cell and a sector of said second non-  
volatile memory on same location of said sector of said first



non-volatile memory indicated by said first address includes an error memory cell.

10. (Previously Presented) A memory controller as defined in Claim 8, further comprising:

an ECC circuit for adding an error detection code to write-data written into said plurality of non-volatile memories to perform an error detection and correction for read-data from said plurality of non-volatile memories,

wherein said ECC circuit performs an input/output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of the parallel access operations.

11. (Previously Presented) A memory controller as defined in Claim 9, further comprising:

an ECC circuit for adding an error detection code to write-data written into said first and second non-volatile memories to perform an error detection and correction for read-data from said first and second non-volatile memories,

wherein said ECC circuit performs an input/output operation at an operation frequency which is equal to an input/output operation frequency of said parallel access operated non-volatile memories multiplied by a number of the parallel access operations.

12. (Original) A memory controller as defined in Claim 8, wherein said memory controller is formed on one semiconductor chip.

13. (Currently Amended) A memory card comprising:  
a control circuit;  
a plurality of non-volatile memories;  
an external interface circuit connected to an external device; and

a bus, wherein  
each of said plurality of non-volatile memories has management information used for performing an address substituting process thereon, said address substituting process being performed individually for each of said plurality of non-volatile memories;

said plurality of non-volatile memories have a plurality of input/output terminals;

said bus has a first bit width, is divided into each of bits having a predetermined number, and is connected to the input/output terminal of a corresponding one of said plurality of non-volatile memories; and

said control circuit performs an access control to said plurality of non-volatile memories by issuing addresses, of which a first address is for a first non-volatile memory and a second address of which is for a second non-volatile memory,

and performs said address substituting process on each of said plurality of non-volatile memories when an access error occurs,

wherein said control circuit is adapted to ~~access a first~~ issuing said addresses, such that said first address of a ~~first non-volatile memory and said first second address of a~~ second non-volatile memory in parallel indicate same location ~~sectors,~~ when both of said ~~first address sector~~ of said first non-volatile memory indicated by said first address and said ~~first address sector~~ of said second non-volatile memory indicated by said second address do not include an error memory cell, and

wherein said control circuit is adapted to ~~access a~~ second ~~issuing said addresses, such that said first address of~~ said first non-volatile memory and a third said second address ~~of said second non-volatile memory in parallel indicate~~ different location sectors, when a ~~second address said sector~~ of said first non-volatile memory indicated by said first address does not include an error memory cell and a sector of said third second non-volatile memory on same location of said sector of said first non-volatile memory indicated by said first address includes an error memory cell.

Claims 14-15 (Cancelled).